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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,130	02/28/2002	Nikki M. Bruner	P1569US01	4401

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EXAMINER	
TORRES, JOSEPH D	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,130	BRUNER ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/28/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference character(s) mentioned in the description: '230' in line 27 on page 12. Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: '308' in Figure 11. Corrected drawing sheets, or amendment to the specification to add the reference character(s) in the description, are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled

"Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 15-20 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Schachner; Joseph M. et al. (US 6442730 B1, hereafter referred to as Schachner).

35 U.S.C. 102(e) rejection of claims 1, 15-17 and 27.

Schachner teaches an apparatus, comprising: a digital data channel which stores input data to a recordable medium and subsequently retrieves readback data from the medium corresponding to the input data (Col. 2, lines 1-4 in Schachner teaches an automated disk drive analysis apparatus and method in which the PRML signal can be analyzed at any point in the disk drive from the pre-amp stage through output channel;

Note: a disk drive is a digital data channel which stores input data to a recordable medium and subsequently retrieves readback data from the medium corresponding to the input data); and an emulation circuit, connected to the digital data channel (col. 5, lines 19-22 of Schachner teaches a Disk Drive Failure Analysis DDFA apparatus with channel emulation capabilities, hence the Disk Drive Failure Analysis DDFA apparatus in Schachner is an emulation circuit, connected to the digital data channel), which arranges the input data into an input sequence of multibit symbols each having a first selected symbol length and arranges the readback data into an output sequence of multibit symbols each having the first selected symbol length (col. 5, lines 37-54 in Schachner teaches a reference signal is selected as an input sequence for comparing with readback data to track errors byte-by-byte; Note: a byte is a multibit symbol), wherein the emulation circuit determines a number of erroneous symbols in the output sequence in relation to differences between the input sequence and the output sequence to predict error rate performance of the digital data channel (col. 5, lines 37-54 in Schachner teaches that DDFA emulation circuit apparatus determines a number of erroneous symbols in the output sequence in relation to differences between the input sequence and the output sequence to predict error rate performance of the digital data channel; Note: col. 10, lines 55-56 in Schachner teaches that the number of errors are found and displayed and col. 4, lines 32-37 in Schachner teaches that the Sequence Amplitude Margin is used to predict error rate) using a first error correction code (ECC) encoding methodology based on the first selected symbol length (col. 23, lines 29-42 in Schachner teaches the NRZ probe of the DDFA emulation circuit

apparatus uses a first error correction code ECC to detect errors; Note: an ECC is inherently based on symbol length and the amount of redundancy required to provide reliable transmissions over noisy channels for the particular symbol length).

35 U.S.C. 102(e) rejection of claims 2 and 18.

Figure 14 in Schachner teaches the NRZ probe in the DDFA emulation circuit apparatus comprises a memory having a first memory location (Ref Mem 1422 in Figure 14 of Schachner) and a second memory location (NRZ Mem 1428 in Figure 14 of Schachner), wherein the input data are stored in the first memory location (Ref Mem 1422 in Figure 14 of Schachner) and the readback data are stored in the second memory location (Ref Mem 1422 in Figure 14 of Schachner).

35 U.S.C. 102(e) rejection of claims 3, 19 and 20.

Claims 3 and 19 substantially recite the same steps as in claims 1 and 15-17 for a second input sequence with a second symbol length. Col. 19, lines 28-32 in Schachner teaches that block size is user specified, hence the NRZ probe in the DDFA emulation circuit apparatus in Figure 14 of Schachner is capable of predicting error rate using a second input sequence with a second symbol length different from the first.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 4, 6, 8, 9, 11, 12, 23, 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schachner; Joseph M. et al. (US 6442730 B1, hereafter referred to as Schachner).

35 U.S.C. 103(a) rejection of claim 4.

Schachner substantially teaches the claimed invention described in claims 1-3 (as rejected above).

However Schachner does not explicitly teach the specific use of a FPGA.

The Examiner asserts that FPGAs are a common means for implementing digital circuitry and one of ordinary skill in the art at the time the invention was made would have been highly motivated to use FPGAs because of their flexibility.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Schachner by including use of a FPGA.

This modification would have been obvious to one of ordinary skill in the art, at the time

the invention was made, because one of ordinary skill in the art would have recognized that use of a FPGA would have provided the opportunity to implement a flexible embodiment of the DDFA emulation circuit apparatus taught in the Schachner patent.

35 U.S.C. 103(a) rejection of claim 6.

Schachner substantially teaches the claimed invention described in claims 1-4 (as rejected above).

However Schachner does not explicitly teach the specific use of the number of erroneous symbols in the output sequence in relation to a total umber of said symbols greater than a first selected number of erroneous symbols that can be corrected by the first error correction code (ECC) encoding methodology.

The Examiner asserts that Figure 14 of Schachner teaches a comparator for detecting errors independently of ECC so that use of the number of erroneous symbols in the output sequence in relation to a total umber of said symbols greater than a first selected number of erroneous symbols that can be corrected by the first error correction code (ECC) encoding methodology is an embodiment of the teachings in Schachner. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Schachner by including use of the number of erroneous symbols in the output sequence in relation to a total umber of said symbols greater than a first selected number of erroneous symbols that can be corrected by the first error correction code (ECC) encoding methodology. This modification would have been obvious to one of ordinary skill in the art, at the time the

invention was made, because one of ordinary skill in the art would have recognized that use of the number of erroneous symbols in the output sequence in relation to a total umber of said symbols greater than a first selected number of erroneous symbols that can be corrected by the first error correction code (ECC) encoding methodology would have provided the opportunity to calculate actual error rate of the system.

35 U.S.C. 103(a) rejection of claims 8 and 23.

Schachner substantially teaches the claimed invention described in claims 1-3 and 15-20 (as rejected above). Col. 23, lines 35-42 in Schachner teach an emulation mode for channel emulation.

However Schachner does not explicitly teach the specific use of inhibiting selected operations of the digital circuit block.

The Examiner asserts that the error analysis during emulation is based upon channel emulation, hence it would be obvious to disable the actual channel to prevent channel data from interfering with error analysis.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Schachner by including use of inhibiting selected operations of the digital circuit block. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of inhibiting selected operations of the digital circuit block would have provided the opportunity to prevent channel data from interfering with error analysis.

35 U.S.C. 103(a) rejection of claims 9 and 24.

Schachner substantially teaches the claimed invention described in claims 1-3, 8, 15-20 and 23 (as rejected above).

However Schachner does not explicitly teach the specific use of a programmable microprocessor.

The Examiner asserts that programmable microprocessor are a common means for implementing digital circuitry and one of ordinary skill in the art at the time the invention was made would have been highly motivated to use a programmable microprocessor because of their flexibility.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Schachner by including use of a programmable microprocessor. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a programmable microprocessor would have provided the opportunity to implement a flexible embodiment of the DDFA emulation circuit apparatus taught in the Schachner patent.

35 U.S.C. 103(a) rejection of claims 11 and 26.

See claim 11 in Schachner.

35 U.S.C. 103(a) rejection of claim 12.

Schachner substantially teaches the claimed invention described in claims 1-3 (as rejected above).

However Schachner does not explicitly teach the specific use of a means using state machines for implement the comparator taught in the Schachner patent.

The Examiner asserts that use of state machines to implement a comparator for clocked data is an obvious engineering design choice and one of ordinary skill in the art at the time the invention was made would have been highly motivated to use state machines to implement the comparator in the Schachner patent running at circuit clock speeds.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Schachner by including use of a means using state machines for implement the comparator taught in the Schachner patent.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a means using state machines for implement the comparator taught in the Schachner patent would have provided the opportunity to implement the comparator in the Schachner patent running at circuit clock speeds.

4. Claims 5, 7, 10, 13, 14, 21, 22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schachner; Joseph M. et al. (US 6442730 B1, hereafter referred to as Schachner) in view of Reed; David E. et al. (US 6115198 A, hereafter referred to as Reed).

35 U.S.C. 103(a) rejection of claims 5, 10, 21 and 25.

Schachner substantially teaches the claimed invention described in claims 1-4, 8, 9, 15-20, 23 and 24 (as rejected above).

However Reed does not explicitly teach the specific use of RLL code.

Reed, in an analogous art, teaches use of RLL code (see RLL Encoder 6 in Figure 2 of Reed).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schachner with the teachings of Reed by including use of RLL code. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of RLL code would have provided the opportunity to minimize errors caused by non-linear transition shift.

35 U.S.C. 103(a) rejection of claims 7, 13, 14 and 22.

Schachner substantially teaches the claimed invention described in claims 1-4 and 15-20 (as rejected above).

However Schachner does not explicitly teach the specific use of interleaving.

Reed, in an analogous art, teaches use of interleaving (see Interleaver 100 in Figure 9A of Schachner).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Schachner with the teachings of Reed by including use of interleaving. This modification would have been obvious to one of ordinary skill in the

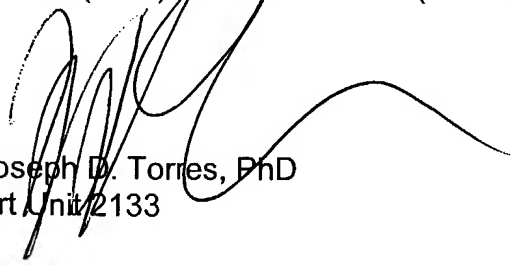
art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of interleaving would have provided the opportunity to effectively decode RLL encoded data.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Art Unit 2133